

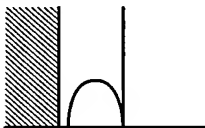
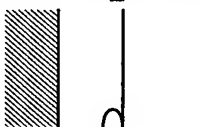
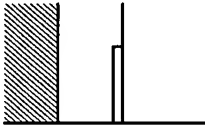
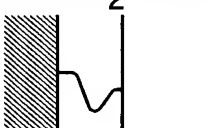

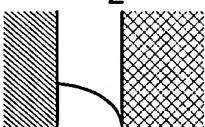
Nitridation Process	[N] Profile	Explanation of the profile	Comments
NO or NO + O <sub>2</sub> Mixture Growth	Gate SiO <sub>2</sub> Sub. 	N Incorporated throughout the film	Poor device performance due to high [N] at the substrate interface
N <sub>2</sub> O Anneal	Gate SiO <sub>2</sub> Sub. 	N close to Si/SiO <sub>2</sub> interface	[N] Content insufficient to block Boron or reduce leakage in 0.1 μm devices
NO Anneal	Gate SiO <sub>2</sub> Sub. 	N at the Si/SiO <sub>2</sub> interface	[N] higher than N <sub>2</sub> O anneal. Traps B inside SiO <sub>2</sub> . Poor interfacial properties and not significant reduction in leakage current
NH <sub>3</sub> Anneal (High Pressure ≥ 100 Torr)	Gate SiO <sub>2</sub> Sub. 	Bimodal [N] distribution. N at the surface & substrate interface	[N] higher than NO anneal. N at surface traps Boron. Poor interfacial properties
Plasma Nitridation	Gate SiO <sub>2</sub> Sub. 	High [N] at the poly/oxide interface	[N] at the surface blocks the Boron. Drive current degrades for ultra-thin dielectrics (< 10 Å)
NH <sub>3</sub> Anneal (Low Pressure ≤ 10 Torr)	Gate SiO <sub>2</sub> Sub. 	Ideal profile. High [N] at the poly/oxide interface	High Drive current than plasma nitridation. Allows EOT scaling < 11 Å.

TABLE 1

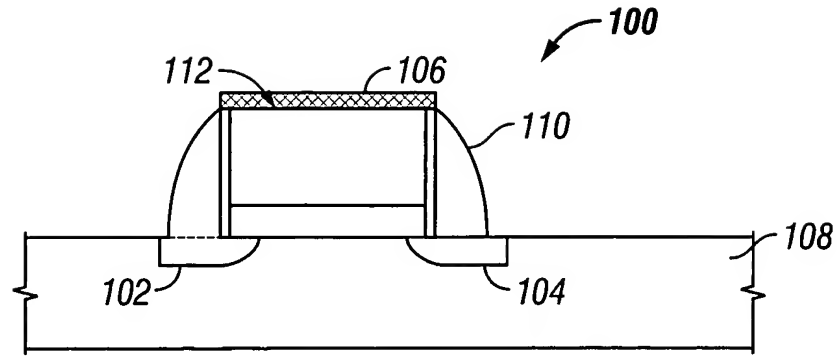


FIG. 1

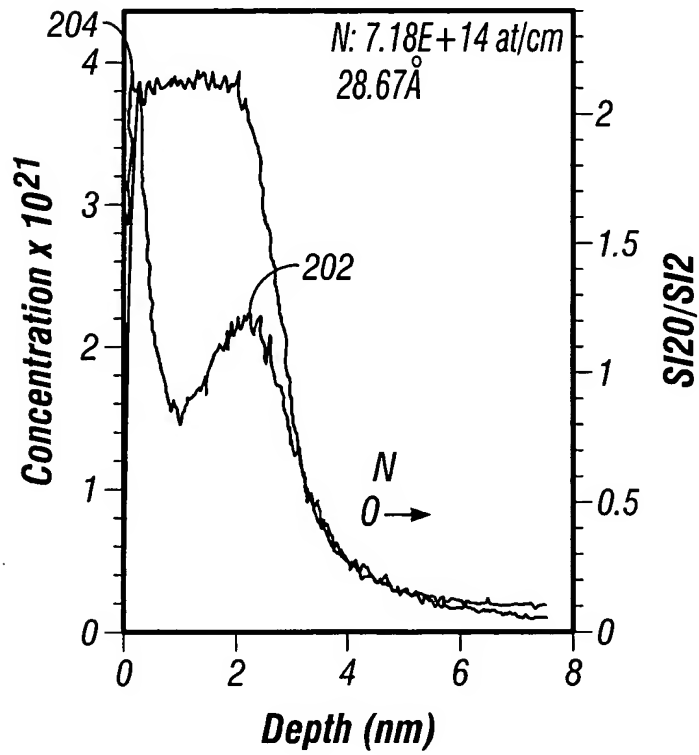


FIG. 2

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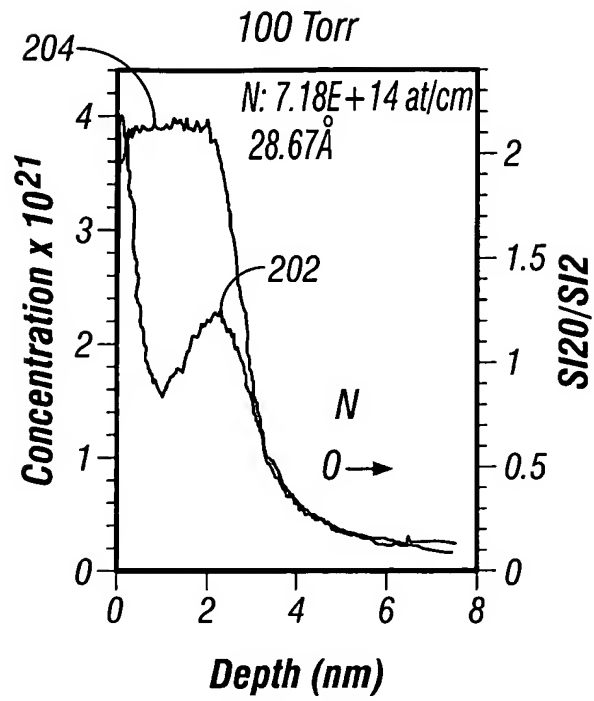


FIG. 3A

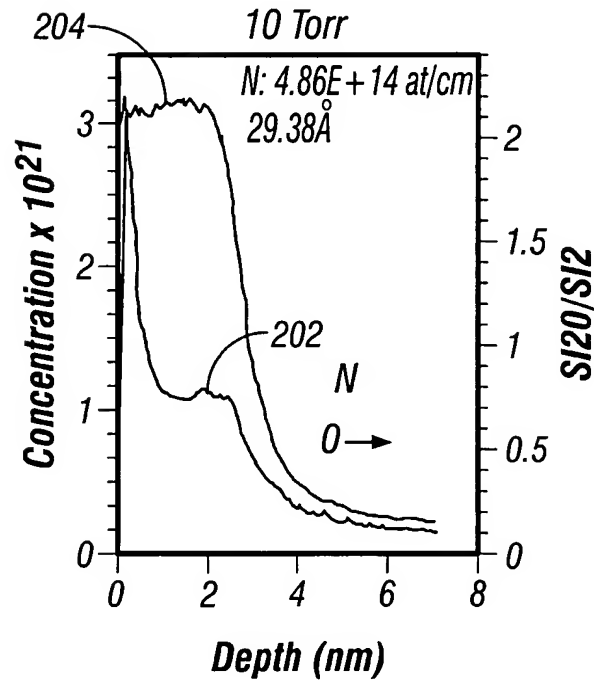


FIG. 3B

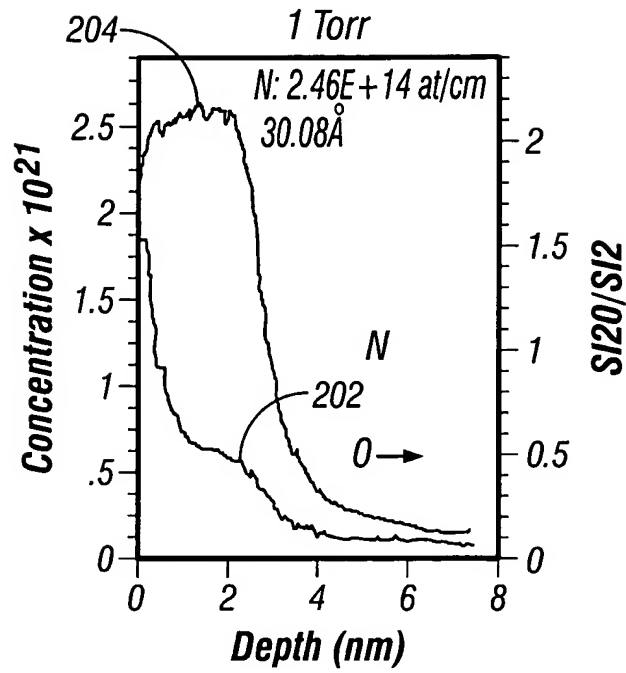


FIG. 3C

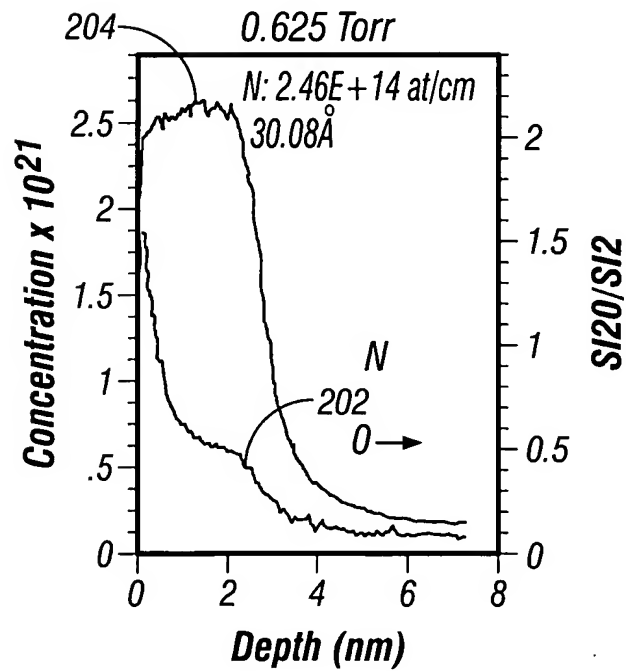


FIG. 3D

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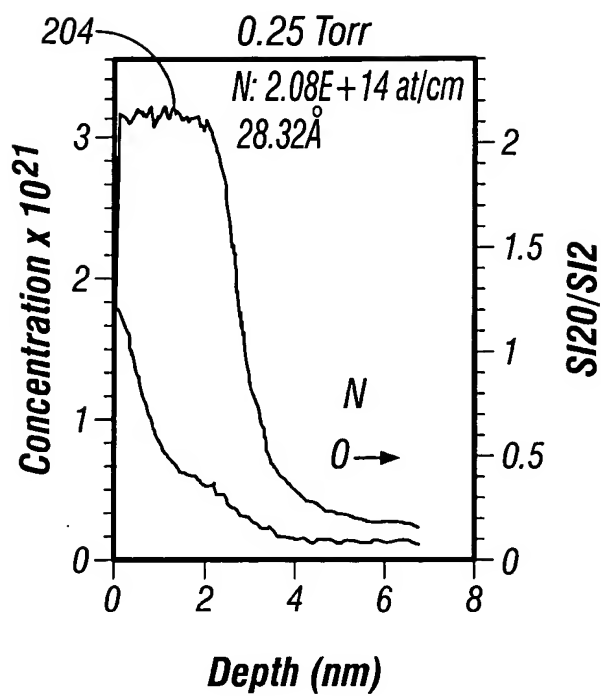


FIG. 3E

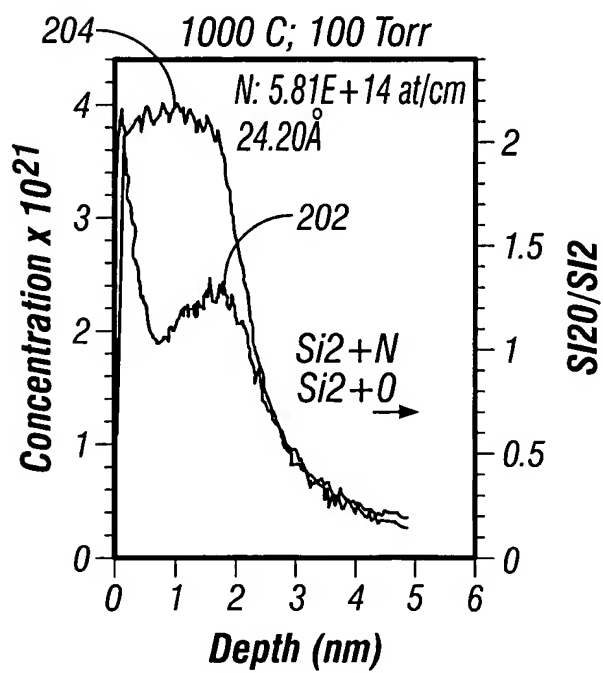


FIG. 4A

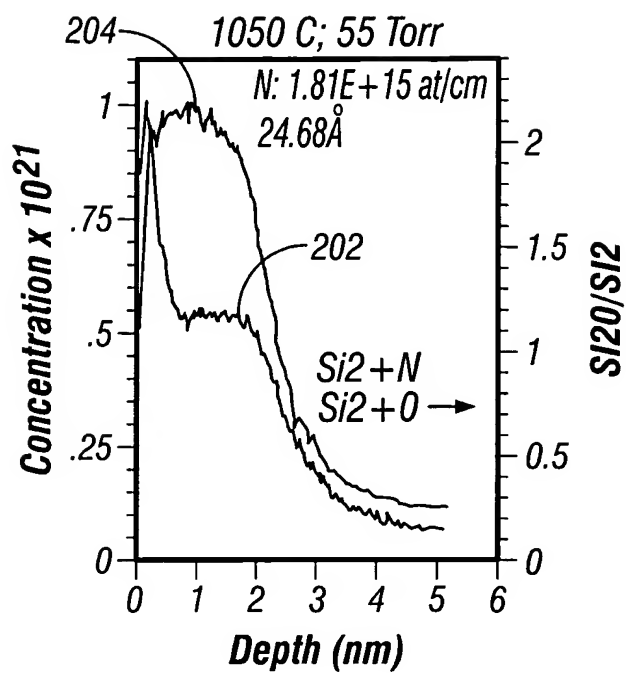


FIG. 4B

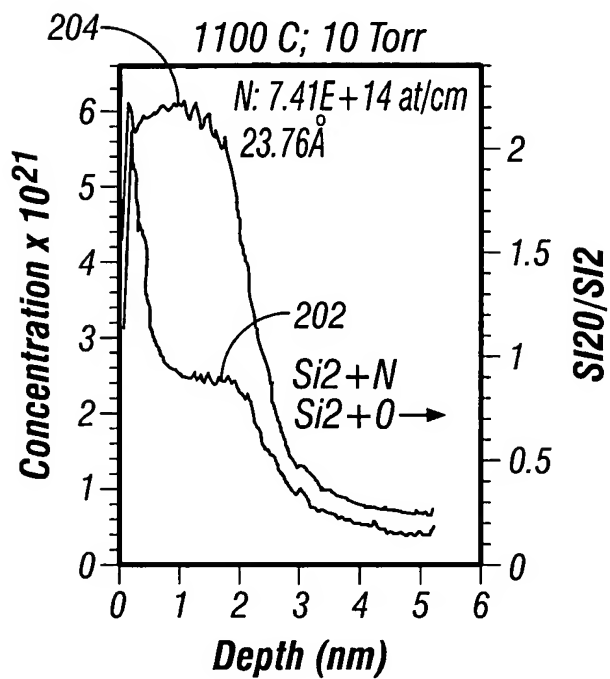


FIG. 4C

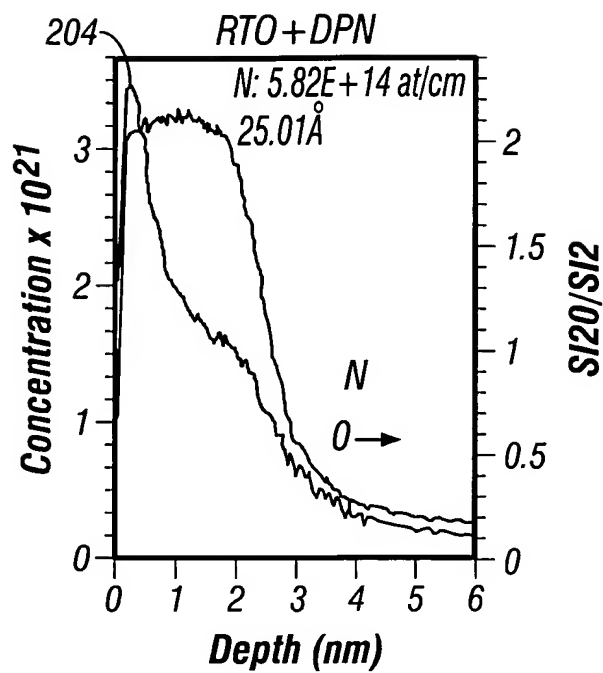


FIG. 5A

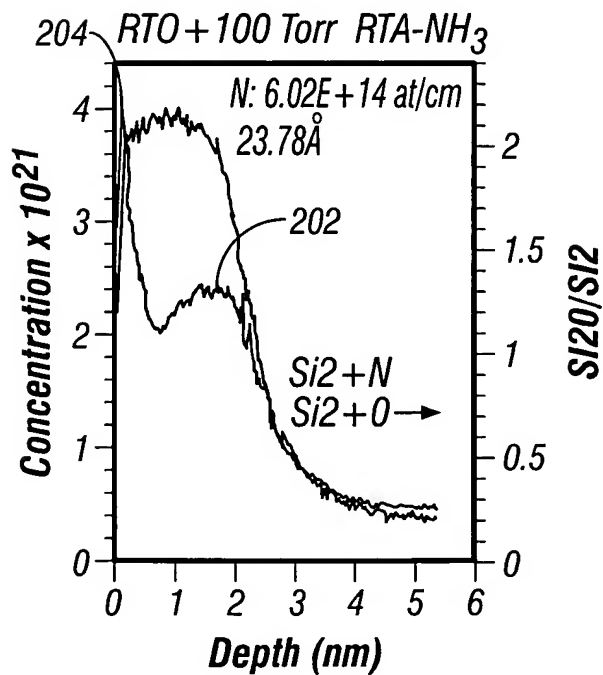
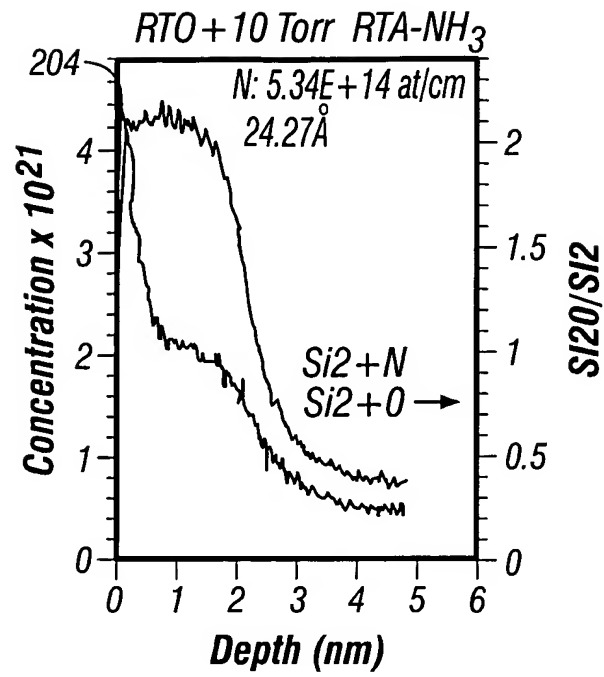
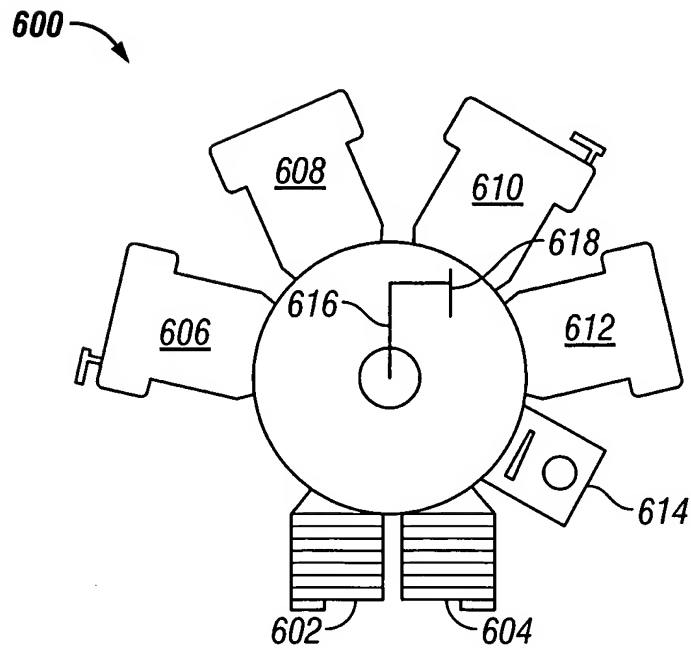


FIG. 5B



**FIG. 5C**



**FIG. 6**